Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A non-volatile memory cell, comprising:
a substrate, having a trench thereon;
a gate, formed within the trench;
a first source/drain region, formed at a bottom of the trench;
a composite dielectric layer, formed between the gate and a surface of the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer; and
a second source/drain region, formed in the substrate on each side of the gate.

[c2] 2. The non-volatile memory cell of claim 1, wherein the gate completely fills the trench.

[c3] 3. The non-volatile memory cell of claim 1, wherein the gate fills the trench and protrudes above the substrate surface.

[c4] 4. The non-volatile memory cell of claim 1, wherein the gate further laterally extend above the substrate outside the trench.

[c5] 5. The non-volatile memory cell of claim 1, wherein the composite dielectric layer also laterally extend above the substrate outside the trench and positioned between the gate and the substrate.

[c6] 6. The non-volatile memory cell of claim 1, wherein the composite dielectric layer further comprises:
a bottom oxide layer, wherein the charge-trapping layer located between the gate and the bottom oxide layer; and
a cap oxide layer, located between the gate and the charge-trapping layer.

[c7] 7. The non-volatile memory cell of claim 1, further comprising spacers formed on the sidewalls of the gate.

[c8] 8. The non-volatile memory cell of claim 7, further comprising a lightly doped region formed in the substrate underneath the spacers.

[c9] 9. The non-volatile memory cell of claim 1, wherein material constituting the gate comprises polysilicon.

[c10] 10. The non-volatile memory cell of claim 1, wherein the composite dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer.

[c11] 11. A method of fabricating a non-volatile memory cell,

comprising the steps of:

providing a substrate;

forming a trench in the substrate;

forming a first source/drain region at a bottom of the trench;

forming a composite dielectric layer in the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer;

forming a gate over the composite dielectric layer within the trench; and

forming a second source/drain region in the substrate on each side of the gate.

[c12] 12. The method of claim 11, wherein the step of forming the trench in the substrate comprises:

forming a patterned mask layer having an opening over the substrate, wherein the opening exposes a portion of the substrate therein;

removing the exposed portion of the substrate to form the trench in the substrate; and

removing the patterned mask layer after forming the first source/drain region at a bottom of the trench but before forming the composite dielectric layer over a sidewall of the trench.

[c13] 13. The non-volatile memory cell of claim 11, wherein the step of forming the composite dielectric layer com-

prises:

forming a bottom oxide layer over the substrate covering a sidewall of the trench;

forming a charge-trapping layer over the bottom oxide layer; and

forming a cap oxide layer over the charge-trapping layer.

[c14] 14. The non-volatile memory cell of claim 11, wherein the step of forming the gate comprises:

forming a conductive layer over the composite dielectric layer, filling the trench;

etching the conductive layer to form the gate; and

removing a portion of the composite dielectric layer outside the gate.

[c15] 15. The method of claim 11, wherein the step of forming the trench in the substrate comprises:

forming a patterned mask layer having an opening over the substrate, wherein the opening exposes a portion of the substrate therein; and

removing the exposed portion of the substrate to form the trench in the substrate.

[c16] 16. The method of claim 15, wherein the step for forming the gate within the trenchcomprises:

forming a conductive layer over the composite dielectric

layer, wherein the conductive layer completely fills the trench and the opening;
removing a portion of the conductive layer and the composite dielectric layer outside the opening; and
removing the mask layer to form the gate.

[c17] 17. The method of claim 11, further comprising a step of forming a device isolation structure for defining an active region in the substrate before the step of forming the trench in the substrate.

[c18] 18. The method of claim 11, further comprising a step of forming a second source/drain region in the substrate on each side of the gate, wherein the step of forming the second source/drain region comprises:
forming a lightly doped region in the substrate;
forming spacers on the sidewalls of the gate; and
forming a heavily doped region in the substrate.